REMARKS

Claims 1, 25, and 32 have been amended, and claim 26 has been canceled herein. Upon entry of this amendment, claims 1, 4, 6, 20-25, and 30-32 will be pending in the above-identified application.

Section 102

Applicant respectfully requests reconsideration of the rejection of Claim 32 under 35 U.S.C. 102(b) as being anticipated by over U.S. Patent No. 4,379,726 (Kumamaru).

Claim 32 recites a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter. The semiconductor device comprises a P-type substrate, an N-type epitaxial layer formed on the substrate, a first embedded diffusion layer formed in a first upper part of the substrate and in the epitaxial layer, and a second embedded diffusion layer formed directly on the substrate, in a second upper part of the substrate, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.

Kumamaru discloses a semiconductor device including a high breakdown voltage element region 13 formed within an N-type epitaxial layer 11 and a P-type epitaxial layer 5, and a buried layer 14 formed in the P-type epitaxial layer 5 and the N-type epitaxial layer 11. The semiconductor device also includes an emitter 19 formed within the high breakdown voltage element region 13 and an emitter 23 formed over the buried layer 14.

Kumamaru does not disclose or suggest a semiconductor device *comprising a P-type substrate, an N-type epitaxial layer* formed on the substrate, and a first embedded diffusion layer formed in a first upper part of the *P-type* substrate and in the *N-type*

epitaxial layer, as recited in claim 32. Rather, in contrast to claim 32 Kumamaru discloses a high breakdown voltage element region and a buried layer, each formed within an N-type epitaxial layer and a P-type epitaxial layer.

Additionally, Kumamaru does not disclose or suggest a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter, and comprising a first embedded diffusion layer and a second embedded diffusion layer, *wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.* As shown in Figure 10 of Kumamaru, the distance between a top of the high breakdown voltage element region 13 and the emitter 19 is less than the distance between a top of the buried layer 14 and the emitter 23, while the distance between a bottom of the high breakdown voltage element region 13 and the emitter 19 is greater than the distance between a bottom of the buried layer 14 and the emitter 23. Thus, several features recited in the claim are absent from the cited reference. Accordingly, the Section 102 rejection of claim 32 is improper and should be withdrawn.

Section 103

Applicant respectfully requests reconsideration of the rejection of claims 1, 4, 6, 20-25, 30, and 31 under 35 U.S.C. 103(a) as being unpatentable over Kumamaru in view of U.S. Patent No. 5,151,765 (Yamauchi) or U.S. Patent No. 4,826,780 (Takemoto).

Claims 1, 4, 6, 20-25, 30, and 31 recite a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter. The semiconductor device comprises a P-type substrate, an N-type

epitaxial layer formed on the substrate, a first embedded diffusion layer formed in a first upper part of the substrate and in the epitaxial layer, and a second embedded diffusion layer formed directly on the substrate, in a second upper part of the substrate, wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.

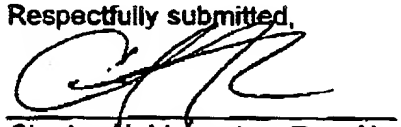
As discussed above, Kumamaru does not disclose or suggest a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor each having an emitter, and comprising a first embedded diffusion layer and a second embedded diffusion layer, *wherein a top of the second embedded diffusion layer is formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between a top of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, and a bottom of the second embedded diffusion layer is formed at a distance from the surface of the emitter of the second vertical type bipolar transistor greater than a distance between a bottom of the first embedded diffusion layer and the surface of the emitter of the first vertical type bipolar transistor.* The secondary references also fail to disclose or suggest these recited features. Thus, the references when considered separately or in combination fail to disclose or suggest several features recited in the claims. Accordingly, the Section 103 rejection is improper and should be withdrawn.

Conclusion

If the Examiner believes that there is any issue which could be resolved by an interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

As it is believed that the application is in condition for allowance, Applicant respectfully requests a favorable action and Notice of Allowance.

Respectfully submitted,



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